REMARKS

The specification has been amended to correct grammatical and typographical errors.

The claims have been amended to correct minor informalities and to address other issues raised by the Examiner.

Claim 7 has been canceled.

Claims 8-11 have been canceled subject to the restriction requirement.

Claims 1-7 were provisionally elected with traverse in response to the telephonic restriction requirement of December 11, 2000.

Claims 1-6 remain pending in the application.

The abstract was objected to as not commencing on a separate page. A new abstract is submitted herewith to satisfy the objection.

The claims were objected to as not having sufficient spacing. Substitute original claims are submitted herewith to satisfy the objection.

Reconsideration and examination of Claims 1-6 in view of the amendments above and the arguments below is respectfully requested.

By way of this amendment, Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain any outstanding issues that require adverse action, it is respectfully requested that Examiner telephone Ralph R. Veseli at (408)433-6404 so that such issues may be resolved as expeditiously as possible.

Claims 1 and 4-6 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Hembree at al. (US 6,121,576)

(Hembree). Applicant traverses the rejection as follows.

The criteria for anticipation under 35 U.S.C. § 102 is set forth at MPEP § 2131, which states:

> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)

The Claims Are Patentably Distinguishable over Hembree

Claims 1 and 4-6 are directed to a thermal profiling device for making accurate temperature measurements at the exact location in an integrated circuit package where a precise temperature is required. Claims 1 and 4-6 recite a packaging substrate having an upper surface, a semiconductor die having an active circuit surface secured to the upper surface of the packaging substrate, and a thermocouple secured to the upper surface of the packaging substrate and to the active circuit surface of the semiconductor die.

As explained in the specification beginning on page 2, line 21, the prior art discloses placing a thermocouple at a location other than the interface between the die and the packaging substrate, i.e., the active circuit surface of the semiconductor die. Applicants have discovered that these devices result in temperature measurements that may vary as much as 10 degrees Centigrade from the actual interface temperature. Applicants also discovered that relying on these inaccurate temperature measurements to control the interface temperature results in the disadvantages of increased chip failure rate and reduced chip reliability.

In FIG. 3 and column 5, lines 25-35, Hembree discloses placing a thermocouple (50) on an upper surface (48)

of a substrate member (18) or on the backside (52) of an insert (16). Both of these locations are separated from the active circuit surface of the semiconductor die by the insert (16), therefore neither of these locations coincides with the interface between the flip chip package (10) and the insert (16).

In contrast to Hembree, Claims 1 and 4-6 recite a thermocouple secured directly to an active circuit surface of the semiconductor die, which is in fact the interface between the semiconductor die and the packaging substrate (see page 5, lines 9-15 of the specification and FIG. 1). Applicants discovered that precise temperature control at the interface is critical, a fact which Hembree does not teach or suggest. Because Hembree does not disclose the location of the thermocouple at the active circuit surface of the semiconductor die as recited in Claims 1 and 4-6 that results in improved chip reliability, Hembree does not show the identical invention in as complete detail as is contained in Claims 1 and 4-6. Because Hembree does not show the identical invention in as complete detail as is contained in the claim, Hembree does not anticipate Claims 1 and 4-6 under 35 U.S.C. § 102.

Claims 2-3 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hembree at al. (US 6,121,576) (Hembree) in view of Hayes (US 5,681,757) (Hayes). Applicant traverses the rejection as follows.

The Claims Are Non-obvious over Hembree and Hayes

As explained above, Hembree does not disclose the claimed securing of a thermocouple directly to the active surface of a semiconductor die. Applicants discovered that

this location is advantageous for precise temperature control, a fact which Hembree does not teach or suggest. Because Hembree does not teach or suggest the advantage of this location as discovered and claimed by Applicants, there is no motivation in Hembree for modifying Hembree to arrive at Claims 2-3.

Hayes is directed to dispensing adhesive, and does not teach or suggest the claimed thermocouple, therefore there is no motivation in Hayes to modify Hembree to arrive at the claimed invention.

Because neither Hembree nor Hayes teach or suggest the claimed thermocouple secured directly to an active surface of the semiconductor die, and because there is no motivation in either Hembree or Hayes to modify Hembree to arrive at the claimed invention, Claims 2-3 are not obvious under 35 U.S.C. § 103(a).

Conclusion

In summary, Claims 1 and 4-6 are not anticipated under 35 U.S.C. § 102(e) by Hembree according to the criteria for anticipation set forth at MPEP § 2131, and Claims 2-3 are not obvious under 35 U.S.C. § 103(a) over Hembree and Hayes.

No additional fee is required for this amendment.

A version with markings to show changes made begins on the following page.

In view of the above, Applicant submits that Claims 1-6 are in condition for allowance, and prompt and favorable action is earnestly solicited.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 7 of page 1 has been amended as follows:

The present invention relates to the field of so-called flip-chip packaging. Flip chip technology is well known in the art of semiconductor packaging, and detailed information concerning flip chip packaging may be found in references such as Microchip Fabrication (3rd Ed.) by Van Zant, P., Chapter 18 "Packaging" (1997) and Ball Grid Array Technology, edited by Lau, John H. (1995), which are hereby incorporated by reference. Some methods of flip-chip packaging use packaging substrates which include one or more bonding pads on one of the substrate surfaces. These bonding pads have a number of circuit connections which will be contacted to a semiconductor chip (or "die"). The die features a plurality of leads which are used to interconnect the die to the packaging substrate. In order to efficiently connect the die to the bonding pad, the leads of the die are treated with tiny lumps of solder ("bumps"), which are used to interconnect the die to other circuit elements, including a bonding pad. Ordinarily, the dies are attached by dipping the die in flux such that the bump surfaces are covered in a small amount of flux. The flux treated die is then carefully aligned and placed on the bonding pads of the packaging substrate. The packaging substrate and die [~~substrates~~] are then placed in a reflow furnace, where the packaging substrate and die are subjected to a carefully controlled temperature process designed to

optimize the bond between the bumps and the bonding pad. This process of heating the bumps to a desired melting temperature to electrically connect the die to the packaging substrate is known as reflowing. Once this reflow process is completed, the packaging substrates and their newly bonded dies are subjected to further processing as needed.

Paragraph beginning at line 5 of page 2 has been amended as follows:

To [~~In order to~~] create a good contact between the die and the bonding pad, the process temperatures must be carefully controlled. A typical attachment process begins by aligning the die to the substrate and tacking it in place with flux. Then the die and packaging substrate are placed in a reflow furnace. For example, multizone reflow furnaces may be used to heat [~~treat~~] the die and package to the required temperatures. In the first zone the die and package are typically preheated to a baseline preheating temperature. Once preheated, the substrate and die are passed into a melt zone, typically maintained at a higher temperature. There the substrate and die are then subjected to a melt temperature which melts the solder bumps creating the bond between the bonding pad and the die. Once this is accomplished, the die and substrate are passed onto a cool down zone of the furnace, which allows the solder to cool without degrading the bond between the die and bonding pad. The temperature of each zone is largely dependent on the type of solder used to form the bumps. Each of these three steps (preheat, melt, and cool down) are very temperature critical requiring accurate thermal calibration of each zone. In the past, these temperatures

were calibrated by a process known as thermal profiling. Thermal profiling is used to monitor a temperature vs. time curve. Although the reflow furnaces themselves are set at a certain temperature, this is not the same as the temperature at the interface between the die and the bonding pad. Since it is the interface temperature that is critical, more accurate measurements of the interface temperature are required. Previously, thermal profiling had been done by placing a die on a packaging substrate, then attaching a thermocouple on top of the die and running the substrate through a preheat, melt, cool down cycle in a reflow furnace. The furnace temperatures were then adjusted until the optimum preheat, melt, and cool down temperatures were measured by the thermocouple.

Paragraph beginning at line 28 of page 2 has been amended as follows:

The inventors have discovered that [~~the thermal profile,~~] using these methods does not accurately profile the temperature at the interface between the die and the bonding pad. The inventors have discovered that the temperatures of the previously used methods can vary as much as 10° C from the actual interface temperature. This leads to sub-optimal bonding of the die to the bonding pad. This increases chip failure rate and reduces chip reliability, and is therefore undesirable.

In the Claims:

Claims 7-11 have been canceled.

Claims 1-6 have been amended as follows:

1.(amended) A thermal profiling device [~~for obtaining an accurate thermal profile of a semiconductor device during processing, said device~~] comprising:

a packaging substrate having an upper surface;

a semiconductor die having an active circuit surface secured directly to the upper surface of the [~~being positioned on said~~] packaging substrate; and

a thermocouple secured directly to the active circuit surface of the semiconductor [~~positioned between said substrate and said~~] die.

2.(amended) The thermal profiling [~~A~~] device of [~~as in~~] Claim 1[~~,~~] wherein the [~~said~~] thermocouple is secured [~~in place between said substrate and said die~~] using an adhesive.

3.(amended) The thermal profiling [~~A~~] device of [~~as in~~] Claim 2[~~,~~] wherein the [~~said~~] adhesive comprises an epoxy.

4.(amended) The thermal profiling [~~A~~] device of [~~as in~~] Claim 1 wherein the [~~said semiconductor die includes an~~] active circuit surface has [~~having~~] electrically conductive bumps formed thereon and the upper surface of the [~~said~~] packaging substrate includes a plurality of bonding pads wherein the [~~formed on a surface thereof, said~~] semiconductor die is [~~being~~] positioned on the [~~said~~] packaging substrate such that the [~~said~~] electrically conductive bumps are in electrical contact with the [~~said~~] plurality of bonding pads.

5.(amended) The thermal profiling [~~A~~] device of [~~as in~~]

Claim 4 wherein the [~~said~~] packaging substrate and the [~~said~~] semiconductor die are secured in place by a solder bond between the [~~said~~] electrically conductive bumps and the [~~said~~] plurality of bonding pads[~~, said bond securing said thermocouple in position between said packaging substrate and said semiconductor die~~].

6.(amended) A thermal profiling device [~~for obtaining an accurate thermal profile of a semiconductor device during processing, said device~~] comprising:

a packaging substrate having a first surface and a second opposite surface;

an opening passing through the second opposite surface and through the first surface of the packaging substrate [~~said first surface including at least one bonding pad~~];

a semiconductor die having an active circuit surface [~~being~~] secured directly to the first surface of the packaging substrate [~~said at least one bonding pad,~~

~~said packaging substrate having an opening in said second opposite surface~~]; and

a thermocouple positioned inside the [~~said~~] opening and secured directly to the active circuit surface of the semiconductor die [~~in place~~].

Substitute Claims (as originally filed):

1. A device for obtaining an accurate thermal profile of a semiconductor device during processing, said device comprising:

a packaging substrate;

a semiconductor die being positioned on said packaging substrate; and

a thermocouple positioned between said substrate and said die.

2. A device as in Claim 1, wherein said thermocouple is secured in place between said substrate and said die using an adhesive.

3. A device as in Claim 2, wherein said adhesive comprises an epoxy.

4. A device as in Claim 1 wherein said semiconductor die includes an active circuit surface having electrically conductive bumps formed thereon and said packaging substrate includes a plurality bonding pads formed on a surface thereof, said semiconductor die being positioned on said packaging substrate such that said electrically conductive bumps are in electrical contact with said plurality bonding pads.

5. A device as in Claim 4 wherein said packaging substrate and said semiconductor die are secured in place by a solder bond between said electrically conductive bumps and said plurality of bonding pads, said bond securing said thermocouple in position between said packaging substrate and said semiconductor die.

6. A device for obtaining an accurate thermal profile of

a semiconductor device during processing, said device comprising:

a packaging substrate having a first surface and a second opposite surface;

said first surface including at least one bonding pad;

a semiconductor die being secured to said at least one bonding pad;

said packaging substrate having an opening in said second opposite surface; and

a thermocouple positioned inside said opening and secured in place.

7. A device as in Claim 6, wherein said opening in said second opposite surface passes through said first surface and said bonding pad.

8. A method of constructing a device for accurately measuring the temperature of a semiconductor device at an interface between a semiconductor die and a packaging substrate, the method comprising the steps of:

a. providing a semiconductor die, said die including an active circuit surface electrically conductive bumps formed thereon;

b. removing said bumps from said semiconductor die;

c. providing a packaging substrate, said substrate including a first surface for receiving said semiconductor die and an opposite second side;

d. providing a thermocouple; and

e. securing the active surface of said die to the first surface of said substrate such that said thermocouple is positioned between the active surface of said die and the first surface of said substrate.

9. A method as in Claim 8, wherein said step e), of securing said thermocouple between said die and said first surface, includes the steps of:

i) treating said thermocouple with epoxy;

ii) contacting the epoxy treated thermocouple to the active surface of said die;

iii) contacting the epoxy treated thermocouple and the active surface of said die to the first surface of said substrate such that said thermocouple is positioned between the active surface of said die and the first surface of said substrate;

iv) clamping said thermocouple in place between the active surface of said die and the bonding pad;

v) curing the epoxy; and

vi) securing said die, said thermocouple, and said substrate in place by soldering said die to said substrate.

10. A method as in Claim 9, wherein said step iv), of clamping said thermocouple between said die and said first surface of said packaging substrate, includes the steps of:

A. providing a stiffener sized to securely fit around said die, said stiffener including a passage sized to pass said thermocouple through said passage;

B. positioning said stiffener on said first surface of said packaging substrate such that the stiffener fits around said die and allows said thermocouple to fit through the passage;

C. providing a heat spreader;

D. clamping said heat spreader in position on said stiffener such that said die, said stiffener, and said thermocouple are all held in place

while said epoxy cures; and

E. after curing the epoxy, removing the heat spreader and the stiffener, leaving the thermocouple epoxied in place between the substrate and die.

11. A method as in Claim 8, wherein said step e), of securing said thermocouple between said die and said first surface of the packaging substrate, includes the steps of:

i) placing said die on the first surface of said substrate such that the electrically conductive bumps of said die are in contact with a plurality of bonding pads formed on said first surface of said substrate; and

ii) reflowing said electrically conductive bumps such that said bumps are secured to said plurality of bonding pads of said substrate to secure said die in place;

iii) forming an opening in said second side of said substrate, said opening passing through said substrate enabling contact with the active surface of said die;

iv) urging said thermocouple into contact with the active surface of said die by inserting said thermocouple into said opening;

v) filling said opening with an epoxy to secure said thermocouple; and

vi) curing the epoxy.